

PATENT ABSTRACTS OF JAPAN

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H01L 21/31
H01L 21/768

(21)Application number : 2001-047358

(71)Applicant : NEC CORP

(22)Date of filing : 22.02.2001

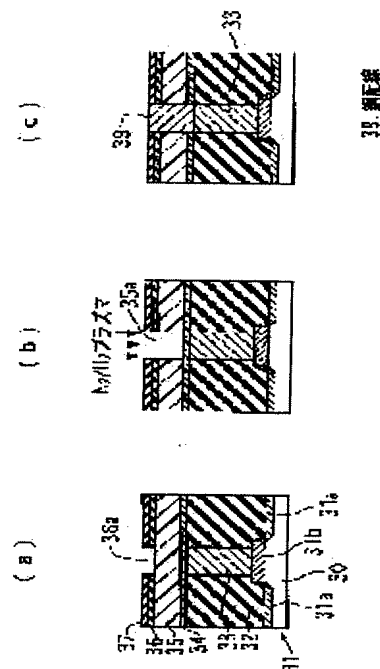
(72)Inventor : OTAKE HIROTO
SAITO SHINOBU
TADA MUNEHIO
HAYASHI YOSHIHIRO

(54) METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE, AND THE SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a technique, with which a plurality of organic films are etched at a high selective ratio.

SOLUTION: The method for manufacturing a semiconductor is provided for etching a non silicon-containing organic film 35, of a combined film composed of a silicon-containing organic film 34 and the non silicon-containing organic film 35, by using mixing gas plasma of nitrogen and hydrogen.



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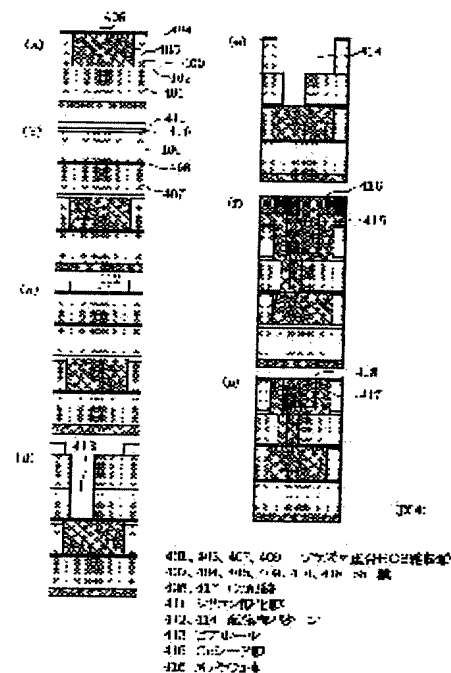
H01L 21/768
H01L 21/312

(71)Applicant : NEC CORP

(72)Inventor : TADA MUNEHIO
HIROI MASAYUKI
KAWAHARA JUN
HAYASHI YOSHIO

PROBLEM TO BE SOLVED: To reduce line resistance, connection resistance and interconnection capacitance while enhancing electromigration resistance by preventing diffusion of copper even if an interconnection trench and a via hole made in an insulation film are directly filled with a metal principally comprising copper.

SOLUTION: An SiN film 406, a BCB(benzocyclobutene) insulation film 407, an SiC film 408, a BCB insulation film 409, an SiC film 410 and an SiO₂ film 411 are deposited on a Cu interconnection 405, a via hole 413 is opened by selective etching (d) and then an interconnection trench 414 is made (e). Subsequently, a Cu seed film 415 is deposited by MOCVD and a Cu film 416 is formed using the Cu seed film as an electrode (f). Excess Cu film is then removed by CMP, a Cu interconnection 417 connected with the Cu interconnection 405 through the via hole is formed, and then an SiC film 418 is formed (g).



PATENT ABSTRACTS OF JAPAN

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C23C 16/30

H01L 21/316

H01L 21/318

H01L 21/768

(21)Application number : 2000-143725

(71)Applicant : NEC CORP

(22)Date of filing : 16.05.2000

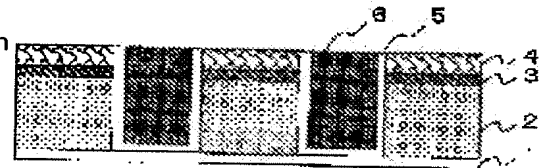
(72)Inventor : USAMI TATSUYA

(54) SEMICONDUCTOR DEVICE, SEMICONDUCTOR WAFER, AND THEIR MANUFACTURING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To improve the interface coherency between low-dielectric-constant and protection films without losing the excellent dielectric characteristics, flatness, and gap fill characteristics of an organic low-dielectric-constant material.

SOLUTION: In wiring structure where a copper film 6 is buried in a wiring layer insulating film, the wiring layer insulating film is in structure where an MSQ(methyl silsesquioxane) film 2, an MHSQ (methylated hydrogen silsesquioxane) film 3, and a silicon oxide film 4 are laminated.



PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-230244

(43)Date of publication of application : 24.08.2001

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B01J 19/08

C08G 61/02

H01L 21/768

(21)Application number : 2000-042209

(71)Applicant : NEC CORP

(22)Date of filing : 21.02.2000

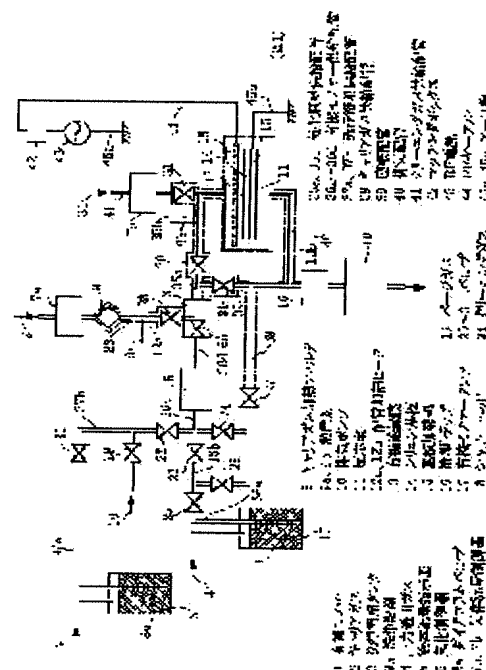
(72)Inventor : KAWAHARA JUN
TADA MUNEHIRO
HAYASHI YOSHIHIRO

(54) METHOD FOR FORMING INSULATING FILM AND MULTILAYER INTERCONNECTION

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a manufacturing method to efficiently grow an insulating film between wiring layers having a high heat resistance and a CMP resistance in forming a low permittivity polymer film on a semiconductor substrate.

SOLUTION: A high heat resistant benzocyclobutene film is efficiently formed by growing a plasma polymer divinylsiloxane bisbenzocyclobutene on a substrate 14 heated to 350° C or higher in a low power plasma of 0.2 W/cm² or less, by vaporizing a divinylsiloxane bisbenzocyclobutene monomer by a vaporization controller 6 and introducing it to a reaction chamber 11. At an initial time of growing, a plasma polymer divinylsiloxane bisbenzocyclobutene film having a relatively small permittivity is grown at a low growing pressure. Then, the growing pressure is increased to continuously grow a dense plasma polymer divinylsiloxane bisbenzocyclobutene film, thereby assuring the CMP resistance by mechanically strengthening a film surface.



PATENT ABSTRACTS OF JAPAN

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(43)Date of publication of application : 12.02.2004

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C23C 14/12
H01L 21/31

(21)Application number : 2002-205468

(71)Applicant : NEC CORP

(22)Date of filing : 15.07.2002

(72)Inventor : HAYASHI YOSHIHIRO

(54) ORGANIC SILOXANE COPOLYMER FILM, ITS MANUFACTURING METHOD, GROWTH APPARATUS, AND SEMICONDUCTOR DEVICE USING SAME

(57)Abstract:

PROBLEM TO BE SOLVED: To provide an insulating organic copolymer film which is suitable for an interlayer dielectric for isolating a multilayered copper wiring of a semiconductor device, is excellent in a mechanical strength and an adhesion in an interface coming into contact with an underlayer or an inorganic insulating film of an upper layer, and has a low effective relative dielectric constant as a whole of the film.

SOLUTION: An annular siloxane and a straight-chain siloxane are used as a raw material, and the both are excited by a plasma and polymerized to form an organic siloxane copolymer film. An interface layer of a film quantity having an excellent minuteness, adhesion is provided in an interface coming into contact with the inorganic insulating film by forming a film composition with a straight-chain siloxane component as a principal component, and an annular siloxane component internalizing a cavity enclosed with a ring-like siloxane frame and a straight-chain siloxane component are mixed. The copolymer film has a layer having a stitch structure suppressing a density relatively and has a composition change in a film thickness direction, and a copper thin film is buried in the copolymer film to form the multilayered wiring.

